Unit 3

Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?  
Data Selector  
Data distributor  
Both data selector and data distributor  
De-Multiplexer

A

Which is the major functioning responsibility of the multiplexing combinational circuit?  
Decoding the binary information  
Generation of all minterms in an output function with OR-gate  
Generation of selected path between multiple sources and a single destination  
Encoding of binary information

C

In a multiplexer, the selection of a particular input line is controlled by \_\_\_\_\_\_\_\_\_\_\_  
Data controller  
Selected lines  
Logic gates  
Both data controller and selected lines

B

 How many select lines would be required for an 8-line-to-1-line multiplexer?  
2  
4  
8  
3

D

How many NOT gates are required for the construction of a 4-to-1 multiplexer?  
3  
4  
2  
5

C

4 to 1 MUX would have \_\_\_\_\_\_\_\_\_\_\_\_  
2 inputs  
3 inputs  
4 inputs  
5 inputs

C

 Most demultiplexers facilitate which type of conversion?  
Decimal-to-hexadecimal  
Single input, multiple outputs  
AC to DC  
Odd parity to even parity

B

In 1-to-4 demultiplexer, how many select lines are required?  
2  
3  
4  
5

A

How many select lines are required for a 1-to-8 demultiplexer?  
2  
3  
4  
5

B

How many AND gates are required for a 1-to-8 multiplexer?  
2  
6  
8  
5

C

Two important characteristics of CMOS devices are \_\_\_\_\_\_\_\_\_\_\_\_  
High noise immunity  
Low static power consumption  
High resistivity  
Both high noise immunity and low static power consumption

D

CMOS technology is used in \_\_\_\_\_\_\_\_\_\_\_\_  
Inverter  
Microprocessor  
Digital logic  
Both microprocessor and digital logic

D

Resistor–transistor logic (RTL) is a class of digital circuits built using \_\_\_\_\_\_\_ as the input network and \_\_\_\_\_\_\_ as switching devices.  
Resistors, bipolar junction transistors (BJTs)  
Bipolar junction transistors (BJTs), Resistors  
Capacitors, resistors  
Resistors, capacitors

A

Which digital system translates coded characters into a more useful form?  
Encoder  
Display  
Counter  
Decoder

D

 A BCD decoder will have how many rows in its truth table?  
10  
9  
8  
3

A

How many possible outputs would a decoder have with a 6-bit binary input?  
32  
64  
128  
16

C

Which one is a basic comparator?  
XOR  
XNOR  
AND  
NAND

A

How many types of digital comparators are?  
1  
2  
3  
4

B

A magnitude comparator is defined as a digital comparator which has \_\_\_\_\_\_\_\_\_\_\_\_  
Only one output terminal  
Two output terminals  
Three output terminals  
No output terminal

C

The purpose of a Digital Comparator is \_\_\_\_\_\_\_\_\_\_\_\_  
To convert analog input into digital  
To create different outputs  
To add a set of different numbers  
To compare a set of variables or unknown numbers

D

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

A > B = 1, A < B = 0, A < B = 1

A > B = 1, A < B = 0, A < B = 1

A > B = 1, A < B = 0, A = B = 0

A > B = 0, A < B = 1, A = B = 1

C

Parity generation and checking is used to detect

which of two numbers is greater

errors in binary data transmission

errors in arithmetic in computers

when a binary counter counts incorrectly

D

Parity generators and checkers use \_\_\_\_\_\_\_\_ gates.

exclusive-AND

exclusive-OR/NOR

exclusive-OR

exclusive-NAND

B

Unit 4

**An active HIGH input S-R latch is formed by the cross-coupling of**

A. Two NOR gates

B. Two NAND gates

C. Two OR gates

D. Two AND gates

A

**Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?**

A. Asynchronous operation

B. Low input voltage

C. Gate impedance

D. Cross coupling

D

**An R-S latch is:**

A. Combinational circuit

B. Synchronous sequential circuit

C. One-bit memory element

D. One clock delay element

C

**When is a flip-flop said to be transparent?**

A. When you can see through the IC packaging

B. When the Q output follows the input

C. When the Q output is opposite the input

D. None

B

**Whose operations are more faster among the following?**

A. Combinational circuits

B. Sequential circuits

C. Latches

D. Flip-flops

A

**The output of latches will remain in set/reset until \_\_\_\_\_\_\_\_\_\_**

A. The trigger pulse is given to change the state

B. Any pulse given to go into previous state

C. They don’t get any pulse more

D. The pulse is edge-triggered

A

**Why latches are called memory devices?**

A. It has capability to store 8 bits of data

B. It has internal memory of 4 bit

C. It can store one bit of data

D. It can store infinite amount of data

C

**Two stable states of latches are \_\_\_\_\_\_\_\_\_\_**

A. A stable and Monostable

B. Low input and high output

C. High output and Low output

D. Low output and high input

C

**When both inputs of SR latches are low, the latch \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

A. Q output goes high

B. Q’ output goes high

C. It remains in its previously set or reset state

D. It goes to its next set or reset state

C

**A flip-flop changes its state during the**

A. Complete operational cycle

B. Falling edge of the clock pulse

C. Rising edge of the clock pulse

D. Both answers (B) and (C)

D

**The truth table for an S-R flip-flop has how many VALID entries?**

A. 1

B. 2

C. 3

D. 4

C

**Like the latch, the flip-flop belongs to a category of logic circuits known as**

(A) Monostable multivibrators

(B) Bistable Multivibrators

(C) Astable Multivibrators

(D) One-shots

B

**On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when \_\_\_\_\_\_\_\_**

a) The clock pulse is LOW

b) The clock pulse is HIGH

c) The clock pulse transitions from LOW to HIGH

d) The clock pulse transitions from HIGH to LOW

C

**What is the hold condition of a flip-flop?**

a) Both S and R inputs activated

b) No active S or R input

c) Only S is active

d) Only R is active

B

**A feature that distinguishes the J-K flip-flop from the S-R flip-flop is the**

(A) Toggle condition

(B) Preset input

(C) Type of clock

(D) Clear input

A

**The race around condition occurs when**

A. J = 0, K = 0

B. J = 0, K = 1

C. J = 1, K = 0

D. J = 1, K = 1

D

**A J-K flip-flop can be made from an S-R flip-flop by using two additional**

A. NAND gate

B. OR gate

C. NOT gate

D. NOR gate

A